Development of frontal anti-reflecting nanotextured silicon layers using electrochemical and chemical etching methods

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Introduction

The aim of this work was to develop and study frontal functional nanolayers of solar silicon (SC) using electrochemical and chemical technologies of porous silicon (PSi) to obtain efficient and cost-effective technological processes for the production of photoelectric converters. These technological processes should be adapted to the processes of production of silicon solar cells. Optimization of the technology of electrochemical formation of porous silicon layers has significantly improved their antireflective and passivation properties. Technologies for creating textures of the SC front surface are based on the process of dissolving the surface layer of silicon in solutions based on hydrofluoric acid. As the surface is covered with Si-O-Si bonds, the dissolution reaction becomes less active and stops with the formation of a continuous oxide film.

As solar energy comes from an unlimited source, the energy capturing process is pollution-free and the technology is established, it stands out amongst the other alternatives as the brightest long-term promise towards meeting the growing demand for energy. One of the more promising methods among the many alternatives is employing solar energy to provide clean auxiliary energy. It is now widely accepted that the rapid reduction of fossil fuel resources together with global warming treaties has necessitated an urgent search for alternative energy sources to partially or completely meet our demands for fossil fuels in the future.

In order for porous silicon to be effectively used as an anti-reflective coating in the structure of silicon SC, its parameters and production technology must meet the following two requirements: a) the parameters of the translucent porous layers should not negatively affect the output electrical characteristics and efficiency of the SC; b) the technological processes of forming and hydrogenating layers of porous silicon should be compatible with the technology of creating silicon SC and not complicate it.

Methods and sample preparation

The first texture, named pyramidal(fig.1), was fabricated by anisotropic etching of Si (100) wafer in a mixed solution of potassium hydroxide (KOH) (9 wt %) and acetic acid (5 vol %) at 75 °C for 10 min. The pyramidal Si samples were then immersed in dilute hydrochloric acid (HCl) for 10 min and hydrofluoric acid (HF) for 5 min to remove any residue KOH and SiO2, respectively. Finally, pyramid-textured Si samples were rinsed with DI water for 20 min at room temperature and dried.

To obtain second sample of pourous silicon surface (fig.2), the research involved the formation of porous silicon layers through electrochemical etching. Monocrystalline (100)-oriented silicon wafers with a specific resistance of 1.5 Ω·cm were used. After chemical cleaning and initial oxidation, a masking oxide was grown at 1050 °C to a thickness of 250 nm, followed by a 30-minute annealing in N2 at 800 °C. Photolithography removed the oxide, and anisotropic chemical etching in a K2CO3-isopropanol solution textured the front surface. HF etching removed the remaining mask. An N+ emitter region, 0.4 μm deep, was formed through phosphorus diffusion from POCl3 source. Thermal treatment at 1050 °C followed HF etching of the phosphorus-silicate glass layer. Finally, a 3 μm Al layer was thermally evaporated as an ohmic contact, annealed in a forming gas (5% H2 in N2) at 450 °C for 20 minutes. The silicon wafers were then diced into 2x2 cm2 samples. Comparatively, electrochemical anodization showed more control and speed than chemical and photo-assisted chemical etching methods, making it suitable for silicon device technology.

For the third sample (fig.3.) to obtain nanowires in our experiments, an open-type CVD setup was used for growing nanoscale crystals. This setup allows for additional doping during the growth process if necessary, provides better control over the size of the nanoparticles (NPs) compared to a closed system, and enables growth without the use of vacuum conditions.

The growth of Si nanocrystals took place by passing a gas mixture of SiCl4 and H2 over a silicon substrate in the reactor at a temperature of 580°C. According to the Vapour-liquid-solid (VLC) growth mechanism , the role of the dopant (metal catalyst) lies in forming a droplet with a relatively low eutectic temperature. The liquid droplet becomes the dominant state for deposition from vapor, leading to supersaturation of silicon in the liquid and its crystallization beneath the droplet. The source of Si, catalyst properties, and the nature of the silicon substrate are crucial for the growth of Si nanocrystals (NCs). In such studies, gold serves as the catalyst since the Au/Si alloy has the lowest eutectic temperature among commonly used metal/Si catalysts, which is a necessary condition for growing thin Si NCs.

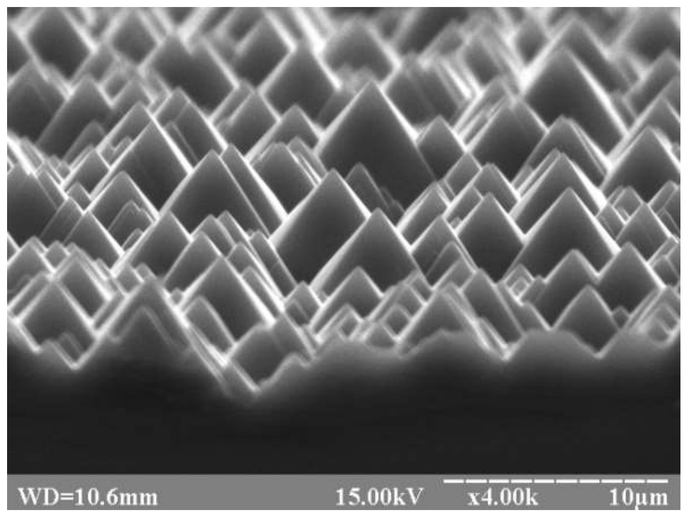

Fig.1 Pyramidal nano surface

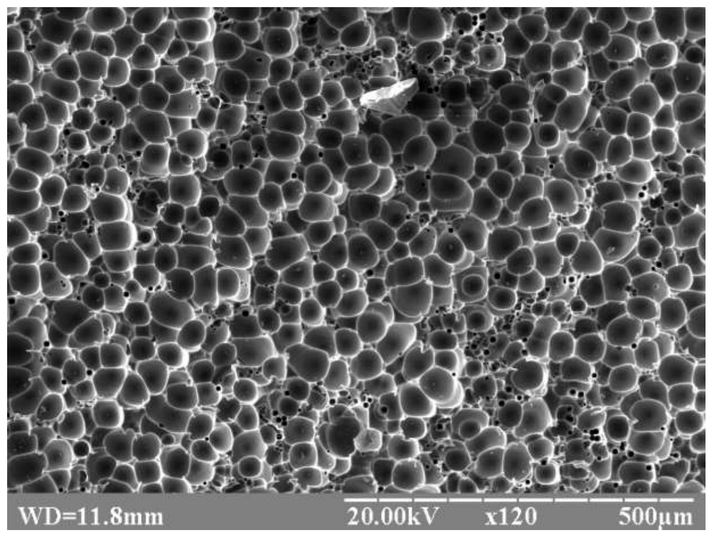

Fig.2 Porous surface

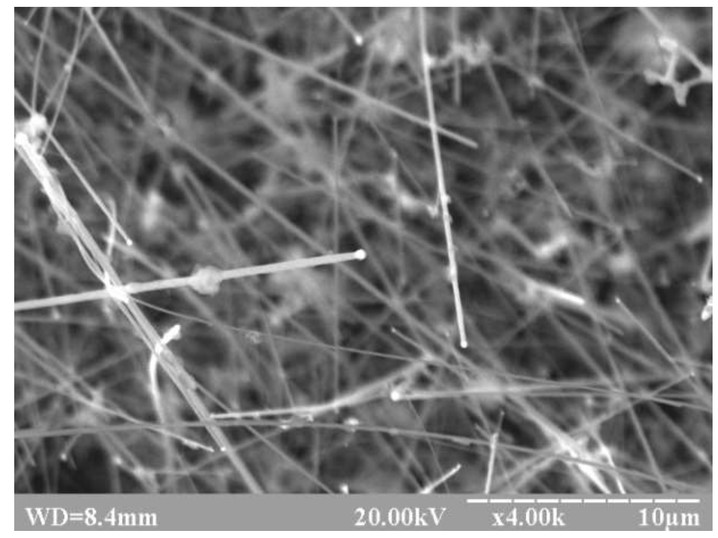

Fig.3 Surface with nanowires

Study of Frontal Functional Nanolayers

Fig.4 Optical reflection of Si samples with various texture:

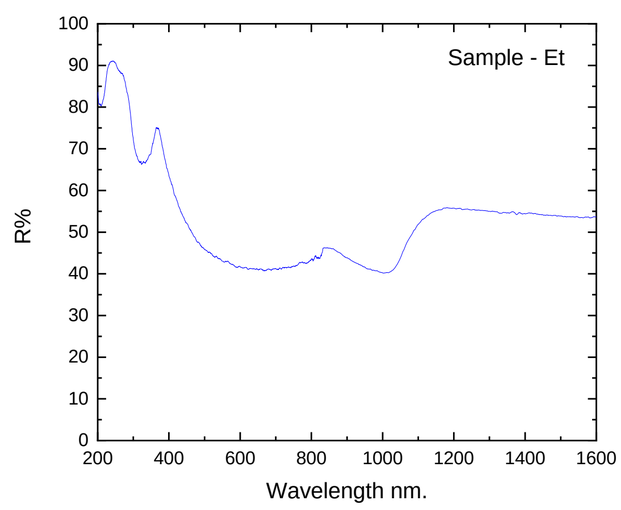

Fig.4a Clean Si wafer

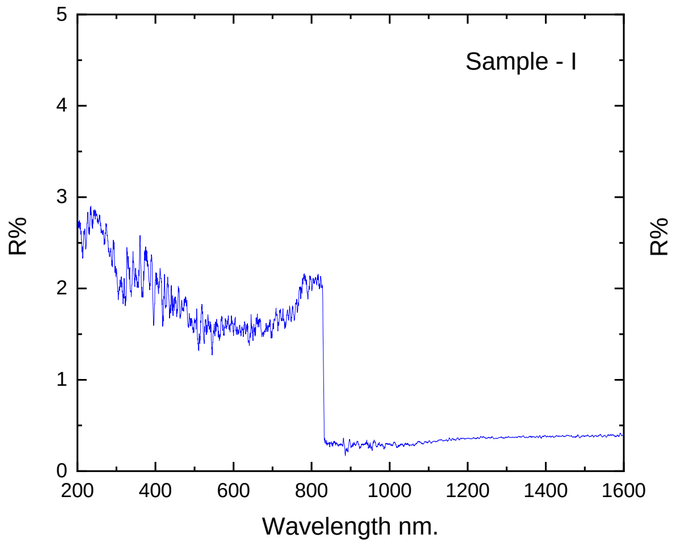

Fig.4b Si wafer with random pyramids

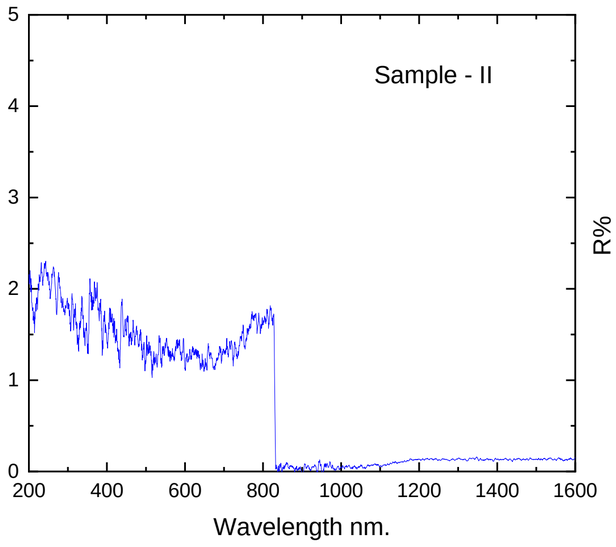

Fig.4c porous Si wafer

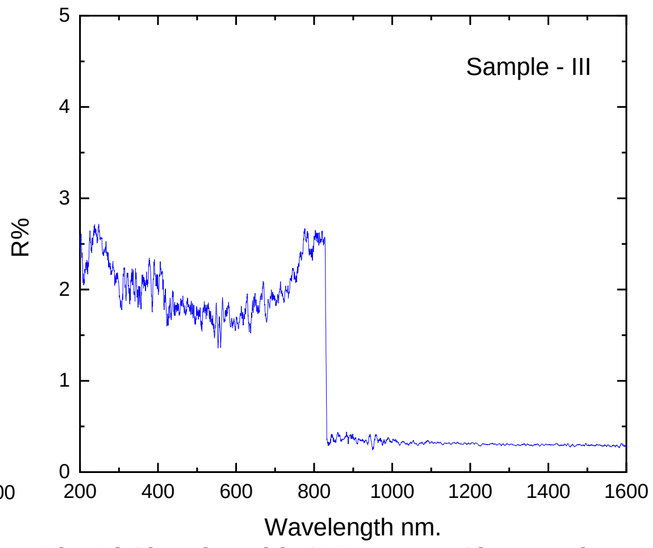

Fig.4d Si wafer with CVD-grown Si nanowires

After obtaining samples, spectroscopic optical investigations were conducted. The collected data is presented in the graphs above. To provide a basis for comparison, an etalon sample (clean Si wafer) was included. In Figure 4, it is evident that the initial silicon wafer sample exhibits a high reflectance factor across the entire wavelength range. In contrast, samples with applied nanostructured layers display the opposite behavior, with reflectance factors lying within the range of up to 5%. Notably, the sample with the porous layer (fig.4c) demonstrates the lowest reflectance among all the tested samples.

Conclusions

In conclusion, our optical investigations have provided valuable insights, with Sample 2, characterized by a porous textured silicon surface, emerging as a standout performer. Remarkably, this sample demonstrated the lowest level of reflection across the spectrum. This finding underscores the substantial potential inherent in porous structures for achieving remarkable optical properties. The exceptional performance of Sample 2 serves as a compelling catalyst for future research endeavors, encouraging deeper exploration of porous textures in silicon and their far-reaching applications in the field of optics.